# Capacitive memory window for non-destructive read operation in ferroelectric capacitors for memory applications

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CMOS back-end-of-line compatible hafnium zirconate (HZO)-based non-volatile ferroelectric (FE) capacitors (FeCAPs) show promise for both random access memory [1] and compute-in-memory applications [2-3]. However, the conventional data reading scheme in FeCAP involves FE polarization switching, which requires re-programming after data reading. Therefore, the read-endurance is limited by the maximum write-endurance, which is, unfortunately, still insufficient for RAM applications. Consequently, decoupling the read- from write-endurance would be beneficial for memory applications. The recently developed concept of a non-volatile capacitive memory window (CMW) promises to enable a non-destructive read operation (NDRO) in FeCAPs to achieve this decoupling [2-5].

The small-signal C-V response of a FeCAP shows a typical FE butterfly motif [6,7]. The positive and negative C-V branches cross at a voltage ($V_{CROSS}$) where the average field in the FE becomes zero. We define the CMW at a read voltage ($V_R \neq V_{CROSS}$) as the difference between the relative dielectric permittivity ($\epsilon_r$) or capacitance values obtained from a FeCAP that was fully pre-polarized in a positive ($P_+$) and negative ($P_-$) polarization state, respectively: $CMW_{\Delta}(V_R) = |\epsilon_+ - \epsilon_-|$ or $|C_+ - C_-|$ [6,8]. In this work, we discuss ways to achieve and improve the CMW followed by the demonstration and understanding of NDRO.

We begin by exploring asymmetry engineering and $V_R$ optimization to realize a non-volatile CMW in a metal-FE-metal (MFM) FeCAP **(Fig. 1(a)-(c))** [6,8]. We then demonstrate that a higher remnant polarization ($2P_R$) in MFM FeCAPs enhances the CMW [9,10]. To further boost the CMW, we integrate a semiconducting IGZO layer into the MFM stack **(Fig. 1(d))** [11]. Using these optimized stacks, we demonstrate NDRO and confirm the decoupling of the read and write endurance in FeCAPs [8,11]. Finally, we investigate the impact of $V_R$ dynamics on NDRO [8,12] and analyze the associated degradation mechanisms.

**References**

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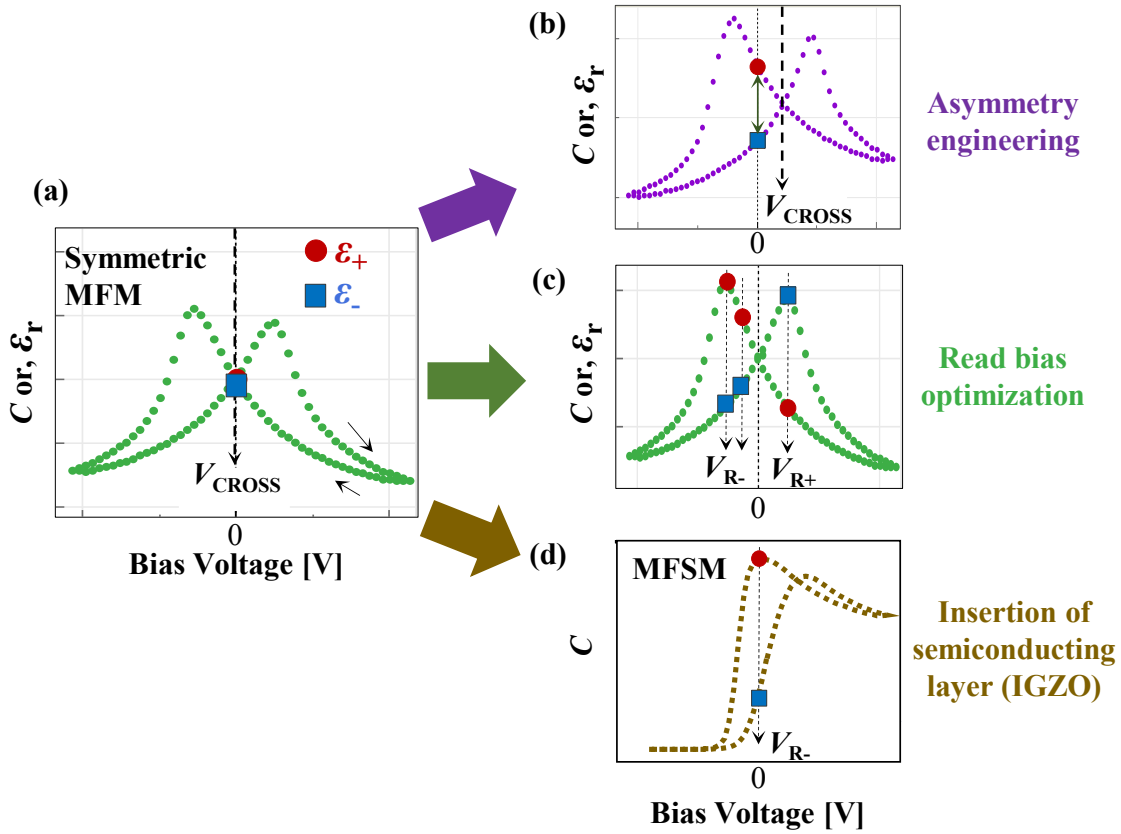


Fig. 1 (a) C-V response of a symmetric FeCAP, where the cross-over ($V_{CROSS}$) happens at 0 V. (b) Asymmetry engineering shifts $V_{CROSS}$ to a non-zero bias so that a non-zero CMW opens up near 0 V. (c) A non-zero CMW can also be realized by reading the capacitive states at a high non-zero $V_R$. However, one needs to optimize the $V_R$ to maintain NDRO. (d) Insertion of a semiconductive layer (such as IGZO) in a MFM stack can improve the CMW. Here, depending on the polarization state of the FE, the semiconductor is either in accumulation or in depletion which further modulates the C-V response of the metal-FE-semiconductor-metal (MFSM) FeCAP and enhances the CMW.